

INTEGRATED CIRCUIT TECHNICAL DATA

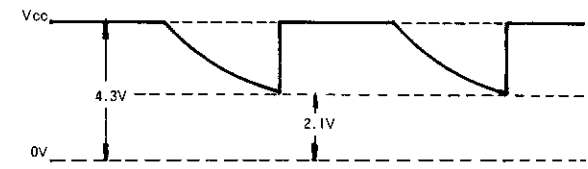
Vol. 2

PA
PD
AN
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FA

- This manual covers the following products.

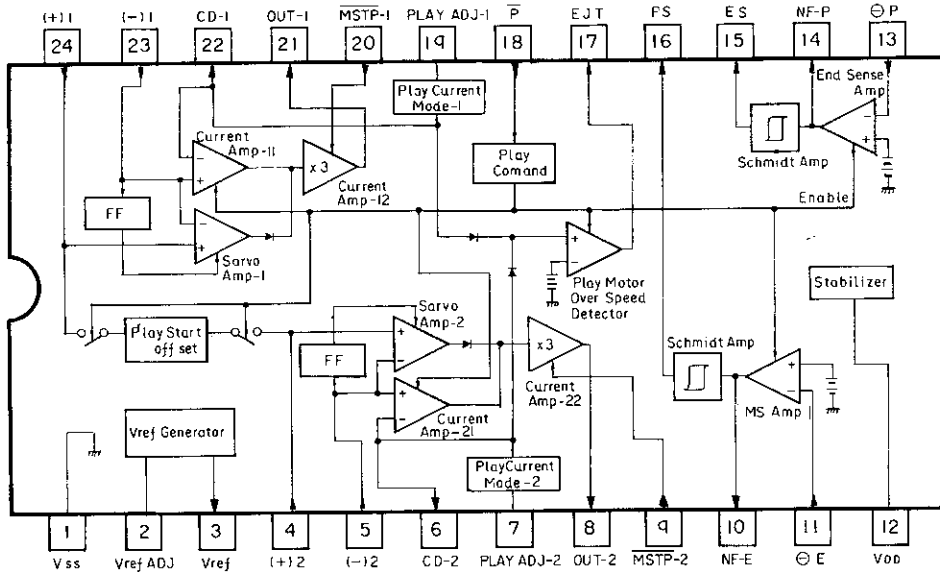
NAME	MODEL	NAME	MODEL	NAME	MODEL	NAME	MODEL
PA 0002A	KP-909G	PD 0002	GEX-60	AN 214	KP-292	BA 328	KH-2277
PA 0003	KP-909G	PD 1002	GEX-8	AN 366	RK-306	BA 1320	RH-4411
PA 2006 (1)	CD-646	PD 1004	SK-700	AN 6550	SK-700	BA 1330	SK-200
PA 3003	GM-40	PD 2001	KP-707G	AN 6913	SK-700	BA 338	KP-404G
PA 3005	GM-4	PD 4003	GEX-8	AN 7146M	SK-51		
PA 3008	GM-D8	PD 6002	KP-707G	AN 7311	SK-51	NAME	MODEL
PA 3009	KP-909G	PD 6009	KP-909G			FA 6013D	KP-333
PA 4007	KEX-70	PD 7001	KE-5000/U. C				
		PD 7002	KE-5000/E				
		PD 7003	GEX-90/US. CA				
		PD 7004	KEX-70/E				

PIONEER ELECTRONIC CORPORATION 4-1, Meguro 1-Chome, Meguro-ku, Tokyo 153, Japan
PIONEER ELECTRONICS (USA) INC. 1925 E. Dominguez St., Long Beach, California 90810 U.S.A.
PIONEER ELECTRONIC (EUROPE) N.V. Keetberglaan 1, 2740 Beveren, Belgium
PIONEER ELECTRONICS AUSTRALIA PTY. LTD. 178-184 Boundary Road, Braeside, Victoria 3195, Australia

Pin No.	Pin Name	Standard Voltage (V)	I/O	Function and Operation
9	CG			Sampling waveform time constant setting 
10	NC			No connection
11	CH			Hold capacitor connection (Note) Since this pin is high impedance, the speed changes when touched with a probe.
12	FV OUT	2.2	OUT	0 dB buffer amp output for CH pin
13	GND			GND
14	NC			Not connected.
15	IN	2.2	IN	Input of buffer amp used by active filter. Buffer amp output terminal.
16	OUT	2.2	OUT	Buffer amp output terminal.

APPLICATION	REEL MOTOR CONTROL & MUSIC SEARCH	NAME	PA0003
MODEL	KP-909G	TYPE	SILICONE MONOLITHIC BIPOLAR DIGITAL IC

BLOCK DIAGRAM



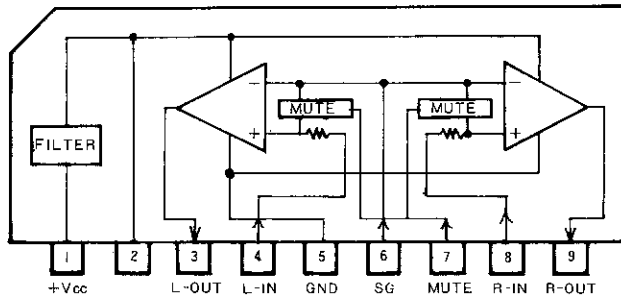
PIN FUNCTIONS

Pin No.	Pin Name	Standard Voltage (V)	I/O	Function and Operation
1	Vss			GND
2	VrefADJ	8.6 ~ 9.3		The three-pin output current is set by an external resistor.
3	Vref	→	OUT	Supplies a constant current to a bridge circuit and produces speed reference voltage Vref. (PLAY, MS modes: $6.9 \pm 1.0V$) (FF, REW Modes: 8.5 ~ 9.3V)
4	(+) 2	→	IN	Servoamp univerted input (corresponds to forward motor) PLAY mode: $4.2V \pm 0.2V$ MS, FF, REW modes: 2-8V change (proportional to tape)
5	(-) 2	→	IN	Servoamp inverted input (corresponds to forward motor) (Operating waveform and voltage are equal to (+) 2 pin)
6	CD-2	→	OUT	Constant current flows in an external resistance in the PLAY Mode. PLAY mode: $4.2V \pm 0.2V$
7	PLAY ADJ-2	→		Sets the motor current in the PLAY mode by external resistor. PLAY mode: 0.7 ~ 1.0V constant, MS, FF, REW modes: 2.5 ~ 4.8V

Pin No.	Pin Name	Standard Voltage (V)	I/O	Function and Operation
8	OUT-2	→	OUT	Drives the base of the forward motor drive transistor. PLAY mode: 2.5 ~ 4V; MS, FF, REW Modes: 2.5 ~ 4.8V
9	$\overline{\text{MSJP-2}}$	→	IN	Forward motor STOP input Motor STOP Mode: 0V Motor RUNNING mode: 0.7 ~ 0.8V
10	NF-E	→	OUT	MUSIC signal amp output. When no MUSIC, approximately 3V constant voltage, when MUSIC, an amplified waveform centered about 3V appears.
11	\ominus E	Approx 3V	IN	Music search MUSIC signal amp input.
12	VDD			Power supply.
13	\ominus P	Approx 3V	IN	END SENSING amp input.
14	NF-P	→	OUT	END SENSING amp output. When the forward & reverse motor stopped, a constant voltage of approximately 3V appears. When both motors or one motor is rotating, a motor ripple voltage amplified waveform appears centered about 3V.
15	PS	→	OUT	END SENSING Schmitt circuit output. When one motor is rotating, an "H" level approximately 6V, "L" level approximately 0V pulse waveform is generated in synchronization with the motor ripple voltage. When both motors are stopped, this pin becomes "H" level
16	ES	→	OUT	MUSIC SENSING schmitt circuit. When music sensed in the PLAY and MS modes, an "H" level approximately 6V, "L" level approximately 0V pulse waveform is generated in synchronization with the music signal. (In all other cases, this pin becomes "H" level.
17	EJT	Normally 0V	OUT	EJECT output when motor races in the PLAY mode. A constant current is output when the motor races in the PLAY mode.
18	$\overline{\text{P}}$	→	IN	PLAY mode switching input. Approx 0V in the PLAY mode. Approx 10V in other modes.
19	PLAY ADJ-1	→		Functions and operation are the same as those of pin 7. Corresponds to the reverse motor.
20	$\overline{\text{MSTP-1}}$	→	IN	Reverse motor stop input. Voltage is the same as that of pin 9.
21	OUT-1	→	OUT	Corresponds to the reverse motor. Functions and operation are the same as those of pin 8.
22	CD-1	→	OUT	Corresponds to the reverse motor. Functions and operation are the same as those of pin 6.
23	(-) 1	→	IN	Corresponds to the reverse motor. Functions and operation are the same as those of pin 5.
24	(+) 1	→	IN	Corresponds to the reverse motor. Functions and operation are the same as those of pin 4.

APPLICATION	ISOLATION AMP	NAME	PA2006 (1)
MODEL	CD-646	TYPE	SILICONE MONOLITHIC BIPOLAR LINEAR IC

BLOCK DIAGRAM

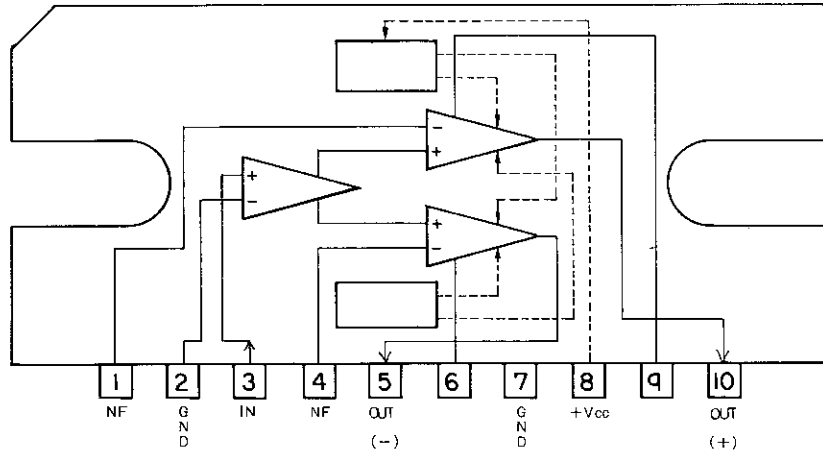


PIN FUNCTIONS

Pin No.	Standard Voltage (V)	I/O	Function and Operation
1	12.6		+Vcc
2	7.6		de-coupling capacitor
3	1.3	OUT	Lch-OUT
4	3.0	IN	Lch-IN
5	0		GND
6	0	IN	SG
7	8.0	IN	MUTE
8	3.0	IN	Rch-IN
9	1.3	OUT	Rch-OUT

APPLICATION	POWER IC	NAME	PA3003
MODEL	GM-40	TYPE	SILICONE MONOLITHIC BIPOLAR LINEAR IC

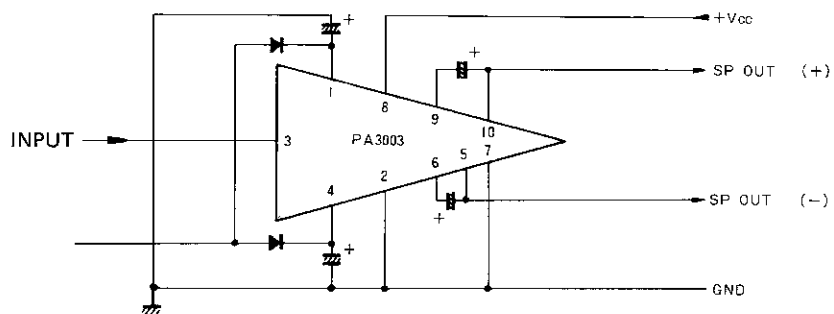
BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Standard Voltage (V)	Function and Operation
1	1.6	NF
2	0	GND
3	0	Input
4	1.6	NF
5	6.9	Output (-)
6	13.2	Boot Strap
7	0	GND
8	13.7	+Vcc
9	13.2	Boot Strap
10	6.8	Output (+)

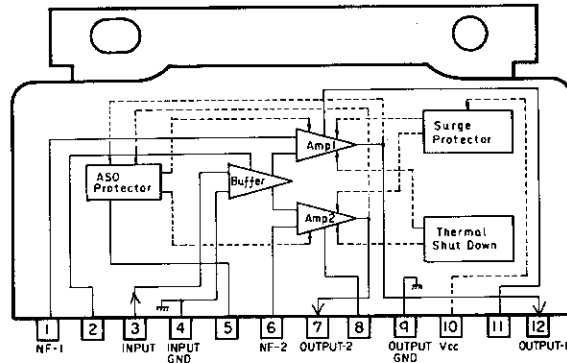
CONNECTION DIAGRAM



PA

APPLICATION	POWER IC	NAME	PA3005
MODEL	GM-4	TYPE	SILICONE MONOLITHIC BIPOLAR LINEAR IC

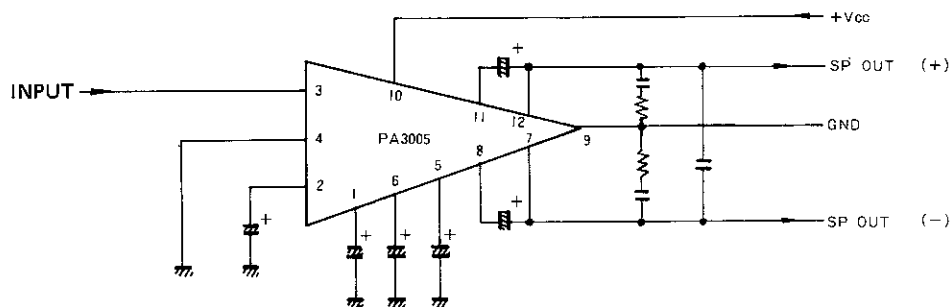
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PIN FUNCTIONS

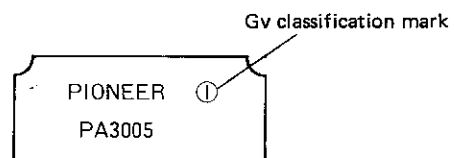
Pin No.	Standard Voltage (V)	Function and Operation
1	1.9	NF
2	3.5	de-coupling
3	0	Input
4	0	GND
5	1.4	ASO protection circuit time constant
6	1.9	NF
7	6.9	Output (reverse phase)
8	13.1	Boot Strap
9	0	GND
10	13.7	+Vcc
11	13.1	Boot Strap
12	6.9	Output (forward phase)

CONNECTION DIAGRAM



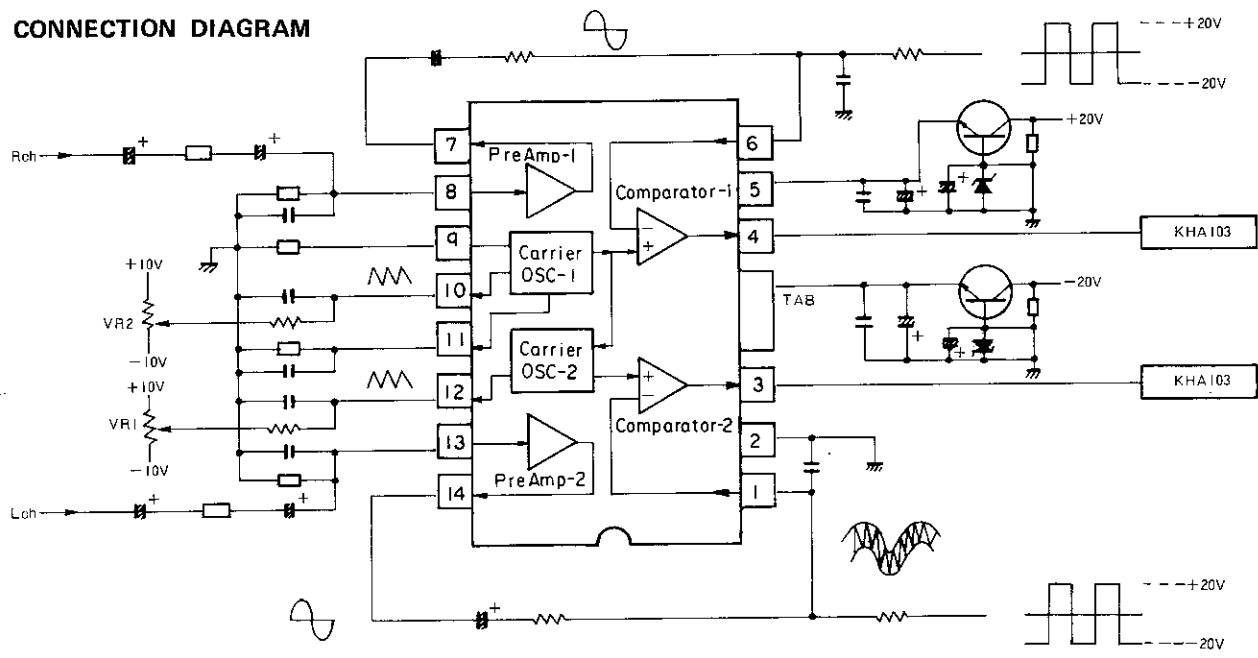
FAMILY

	Voltage gain (Gv)
PA-3005-1	37.5 ~ 39.5
PA3005-2	38.0 ~ 42.0
PA3005-3	40.5 ~ 42.5



APPLICATION	PWM MODULATION	NAME	PA3008
MODEL	GM-D8	TYPE	SILICONE MONOLITHIC BIPOLAR DIGITAL IC

CONNECTION DIAGRAM

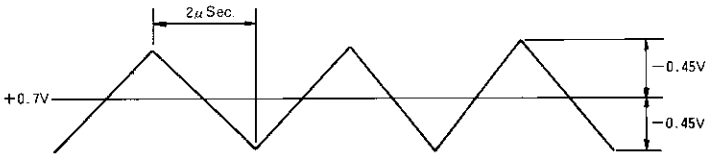
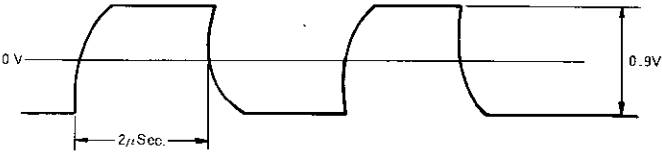


VR1 and VR2 are for triangular wave adjustment.

PIN FUNCTIONS

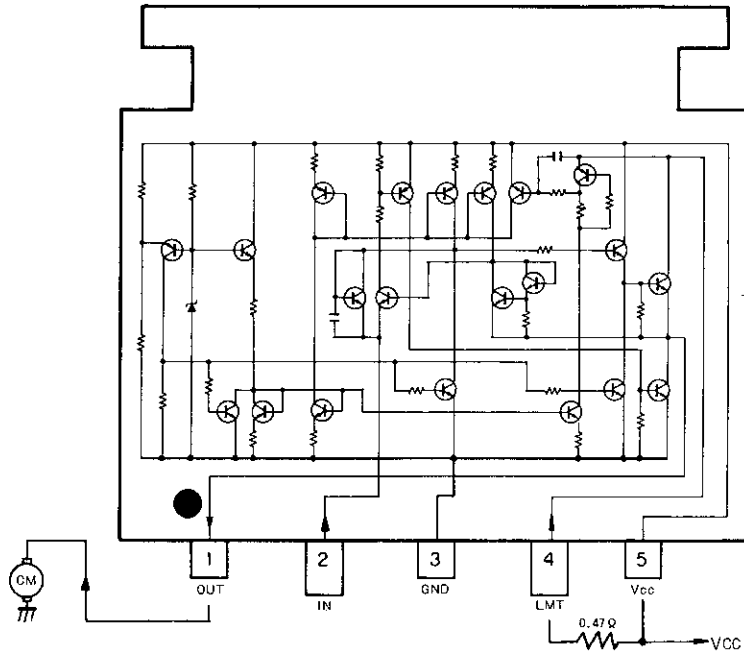
* Waveform are no input signal waveform.

Pin No.	Pin Name	I/O	Function and Operation
1	COMP IN	IN	<p>Comparator input</p>
2	GND		
3	COMP OUT	OUT	<p>Comparator output</p>

Pin No.	Pin Name	I/O	Function and Operation
TAB	-Vcc		Heat sink and -10V.
4	COMP OUT	OUT	Comparator output. Wave height value and waveform are the same as those of pin 3. However, the phase is shifted approximately 60° from that of the output waveform of pin 3.
5	+Vcc		+10V.
6	COMP IN	IN	Comparator input. Wave height value and waveform and the same as those of pin 1. However, the phase is shifted approximately 60° from that of the output waveform of pin 1.
7	PRE OUT	OUT	Outputs a DC voltage of approx +0.1V.
8	PRE IN	IN	Preamp gain 33dB.
9	IR		DC (-5V). Determines the pins 10 and 12 charging and discharging current. Charging and discharging current = $-5.5/12k\Omega$ [mA]
10	OSCI	OUT	<p>Produces a triangular waveform by charging and discharging with a constant current across capacitor terminals.</p> 
11	VH	OUT	<p>Determines the wave height value of pin 10. Outputs a voltage of approximately 0.9V at current determined by pin 9 x 1.8 kΩ</p>  <p>[Pin 10 triangular waveform and phase are matched]</p>
12	OSC2	OUT	Produces a triangular waveform the same as pin 10. However, the phase is shifted approximately 60° from that of pin 10.
13	PRE IN	IN	Preamp gain 33dB.
14	PRE OUT	OUT	Outputs a DC voltage of approximately +0.1V.

APPLICATION	CAPSTAN MOTOR DRIVE	NAME	PA3009
MODEL	KP-909G	TYPE	SILICONE MONOLITHIC BIPOLAR IC

BLOCK DIAGRAM

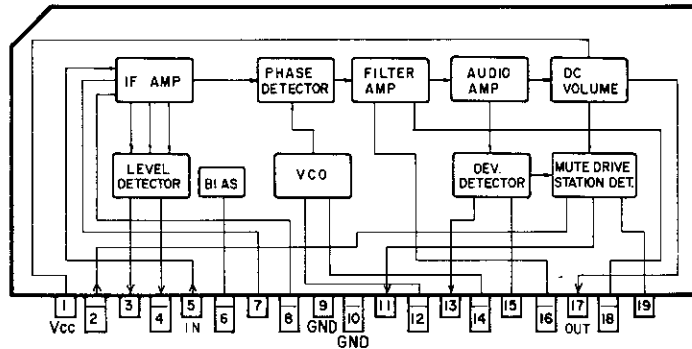


PIN FUNCTIONS

Pin No.	Pin Name	I/O	Function and Operation
1	OUT	OUT	Motor drive output. Operating voltage is 2 ~ 3V At motor starting: 6 ~ 8V At motor stopping: 0V
2	IN	IN	(Current source [approximately 2 ~ 3mA] is connected in the pin 2 direction from Vcc at the inside.) ● Voltage gain between input pin and output pin is 0dB. ● Operating voltage is 0.7V higher than that of the output pin.
3	GND		Ground
4	LMT	IN	Maximum output current setting pin. ● Maximum output current when 0.47Ω connected between pins 4 and 5 becomes 230 ~ 380μA. ● Operating voltage is almost equal to the pin 5 voltage.
5	Vcc		Power supply.

APPLICATION	FM IF SYSTEM	NAME	PA4007
MODEL	KEX-70	TYPE	SILICONE MONOLITHIC BIPOLAR LINEAR IC

BLOCK DIAGRAM



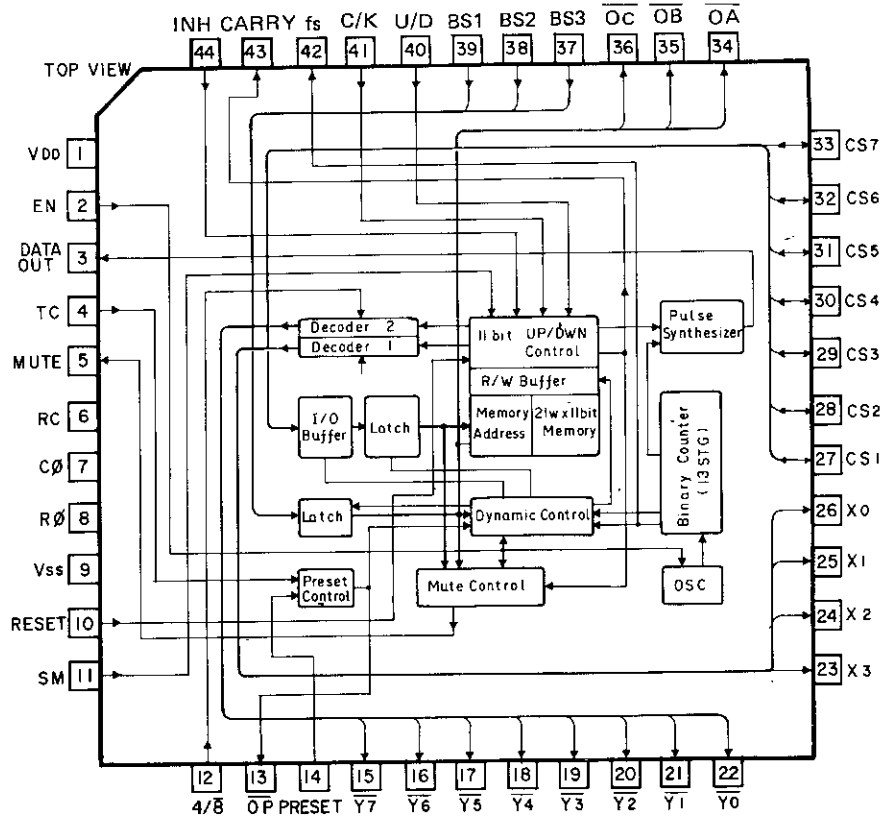
PIN FUNCTIONS

Pin No.	Standard Voltage (V)	I/O	Function and Operation
1	8.5V		Vcc
2	4.9V	IN	Level muting drive input.
3	4.9V	OUT	Signal meter output
4	0	OUT	AGC output
5	2.1V	IN	Input
6	5.8V		Bias
7	2.1V		Input AC ground
8	2.1V		Input AC ground
9	0		GND
10	0		GND
11	0	OUT	Stop pulse output
12	5.1V		VCO
13	5.1V	OUT	AFC output
14	5.1V		VCO AC ground
15	5.1V		Center meter
16	2.8V		Loop filter
17	2.9V	OUT	Output
18	2.8V		Loop filter
19	5.1V		Stop pulse, muting

PA

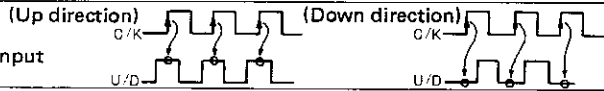
APPLICATION	VOLTAGE SYNTHESIZER	NAME	PD0002
MODEL	GEX-60	TYPE	C MOS

BLOCK DIAGRAM



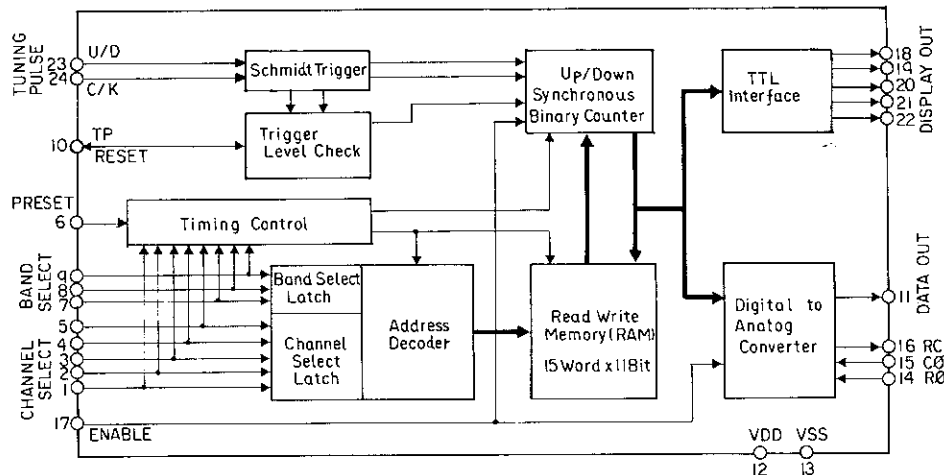
PIN FUNCTIONS

Pin No.	Pin Name	I/O	Function and Operation
1	VDD		+B (8.8V)
2	EN	IN	"L" CLOCK stop. 11 bit up down counter function stop. Dial display. Preset address. Band indicator LED turn off. CARRY, DATA OUT → "L"
3	DATA OUT	OUT	Pulse synthesizer output. Number of pulses depends on the contents of the UP DOWN counter.
4	TC	IN	Preset hold time setting use time constant pin. Normally "H" level.
5	MUTE	OUT	"H" level is output by operating CS1~7, BS1~3 and "H" level is output for 500 msec. when EN "L", "L" level, EN "L → H", "H → L".
6	RC	} Clock oscillation time constant pin.	
7	Cφ		
8	Rφ		

Pin No.	Pin Name	I/O	Function and Operation
9	V _{SS}		GND
10	RESET	} IN	GND at GEX-60.
11	SM		
12	4/8		
13	\overline{OP}	OUT	Not used by GEX-60.
14	PRESET	IN	Preset input. Preset enabled and preset address LED is extinguished simultaneously when H level. (Pull-down resistor built-in.)
15 } 22	$\overline{Y7}$ } $\overline{Y0}$	OUT	Dial display LED drive. (Open drain output)
23 } 26	X3 } X0	OUT	Dial display LED drive.
27	CS1	IN/OUT	Not used by GEX-60. (Pull-down resistor built-in.)
28	CS2		
29 } 33	CS3 } CS7	IN/OUT	Channel select input, address display LED output. (Pull-down resistor built-in.) "H" level . . . Channel select and preset address display.
34	\overline{OA}	} OUT	Band select address LED drive circuit. { Open drain $\overline{OA} \sim \overline{OC}$ outputs corresponding to BS1 ~ 3 become "L" level. }
35	\overline{OB}		
36	\overline{OC}		
37	BS3	} IN	Band select input. (Pull-down resistor built-in.) { Select at "H" level. Corresponding $\overline{OA} \sim \overline{OC}$ output made "L" level. }
38	BS2		
39	BS1		
40	U/D	} IN	Tuning up down input 
41	C/K		
42	f _s	OUT	Not used by GEX-60.
43	CARRY	OUT	
44	INH	IN	

APPLICATION	VOLTAGE SYNTHESIZER	NAME	PD1002
MODEL	GEX-8	TYPE	C MOS

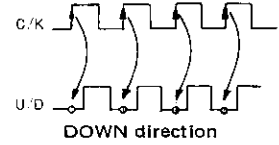
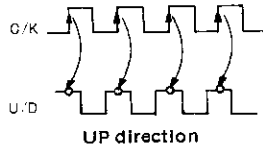
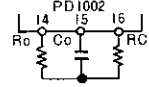
BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Pin Name	I/O	Function and Operation
1	CS1 ~ CS5 CHANNEL SELECT	IN	Station select input used at frequency preset and memory read. Channel selected when "H".
2			
3			
4			
5			
6	PRE SET	IN	Preset enabled by "H" level.
7	BS1 ~ BS3 BAND SELECT	IN	When "H" level, band is selected and a total of 15 BS3 x CS5 stations is possible by combining with channel select.
8			
9			
10	RESET	IN	Contents of UP/DOWN counter are reset by making this pin "H" level. This pin is normally connected to Vss. (Only during inspection.)
11	DATA OUT	OUT	Data output to generate the tuning voltage. Output by pulse waveform and impressed as the tuning voltage through a low-pass filter.

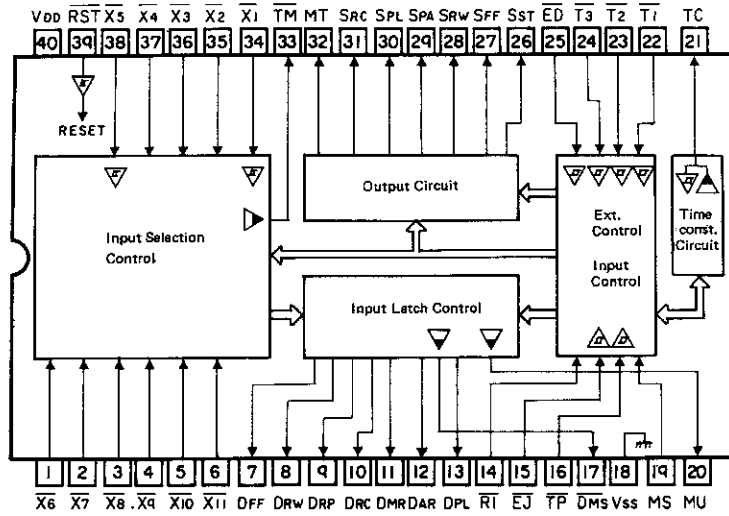
Pin No.	Pin Name	I/O	Function and Operation
12	VDD		System power supply.
13	Vss		System ground.
14	Ro		Determines the oscillation characteristic of the oscillator inside the element. Time constant pin.
15	Co		
16	RC		
17	EN	IN	Controls the operation of the counter and oscillator in the element. Operation is stopped by "L". (ENABLE pin)
18	$\overline{D10} \sim \overline{D06}$	OUT (TTL)	Output of high-order 5 digits of 11 bit UP/DOWN counter. Used for tuning display. EXAMPLE) Tuning display by LED is performed by connecting this pin directly to electronic tuner decoder ID PD4003 pins (1) ~ (5).
19			
20			
21			
22			
23	U/D (UP/DOWN)	IN	Tuning UP/DOWN input. The pulse shown below is input and counter U/D is controlled by turning the turning knob.
24	C/K (CLOCK)	IN	



* PD1002-F is forming type.

APPLICATION	DECK CONTROL	NAME	PD1004
MODEL	SK-700	TYPE	C MOS

BLOCK DIAGRAM



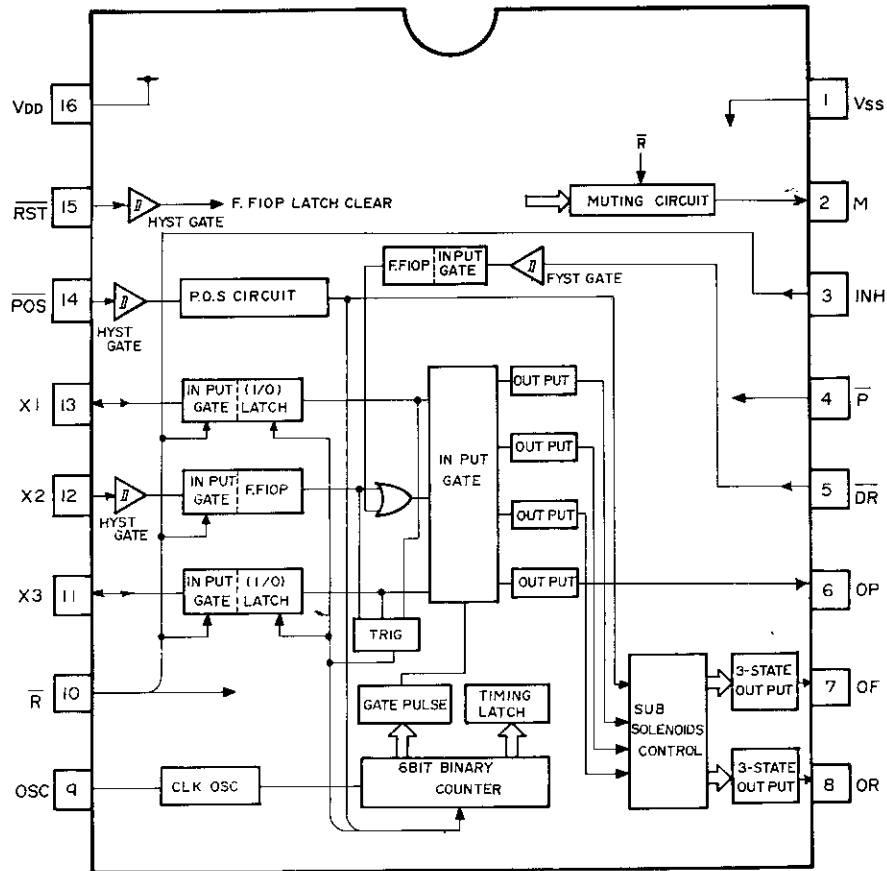
PIN FUNCTIONS

Pin No.	Pin Name	I/O	Function and Operation
1	$\bar{X}6$	IN	REW
2	$\bar{X}7$		REW MS
3	$\bar{X}8$		FF MS
4	$\bar{X}9$		FF
5	$\bar{X}10$		REC
6	$\bar{X}11$		PLAY
7	DFF	OUT	FF
8	DRW		REW
9	DRP		REC PAUSE
10	DRC		REC
11	DMR		MUSIC REPEAT
12	DAR		ONE SIDE REPEAT
13	DPL		TAPE (PLAY)
14	$\bar{R}1$	IN	REC inhibit switch input. REC and REC PAUSE key input is inhibited when this pin is "L".
15	$\bar{E}J$	IN	EJECT switch input. Not used at this time.
16	$\bar{T}P$	IN	TAPE function switch input. TAPE mode when "L".
17	DMS	OUT	FF MS and REW MS display output. Open drain output. Becomes "L" in MS mode.

Pin No.	Pin Name	I/O	Function and Operation	
18	V _{SS}		GND	
19	MS	IN	Interselection detection pulse input.	
20	MU	OUT	Muting signal output. Muting is released and this pin becomes "L" level only in PLAY mode. Open drain output.	
21	TC	OUT	Fall safe pin. The erroneous operation judgement time is set by external CR.	
22	$\overline{T1}$	IN	Mechanism switch input corresponding to STOP operation. "L" when switch ON.	
23	$\overline{T2}$	IN	Mechanism switch input corresponding to PAUSE operation. "L" when switch ON.	
24	$\overline{T3}$	IN	Mechanism switch input corresponding to PLAY, REC, FF, and REW operation. "L" when switch ON.	
25	\overline{ED}	IN	Tape end detection switch input. End of tape is judged by two tape end detection pulses.	
26	SST	OUT	STOP	} Solenoid output
27	SFF		FF	
28	SRW		REW	
29	SPA		PAUSE	
30	SPL		PLAY	
31	SRC		REC	
32	MT	OUT	Motor output.	
33	\overline{TM}	OUT	Time output. Connects to PLAY, REC key input through the timer standby switch.	
34	$\overline{X1}$	IN	STOP	} Key input.
35	$\overline{X2}$		REC PAUSE	
36	$\overline{X3}$		MUSIC REPEAT	
37	$\overline{X4}$		ONE SIDE REPEAT	
38	$\overline{X5}$		REC MUTE	
39	\overline{RST}	IN	Initial reset input.	
40	V _{DD}		+B	

APPLICATION	DECK CONTROL	NAME	PD2001
MODEL	KP-707G, 717G, 818G	TYPE	C MOS

BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Pin Name	I/O	Standard Voltage (V)				Function and Operation
			PLAY	X2 INPUT	X3 INPUT	X1 INPUT	
1	Vss		0	0	0	0	GND.
2	M	OUT	0	12.6	12.4	12.4	Muting output for each input.
3	INH	IN					NC
4	P-bar	IN	0	0	12.4	12.4	Play running direction switching is inhibited by X2 terminal at FF/REW. (Pull-up resistor built-in.)

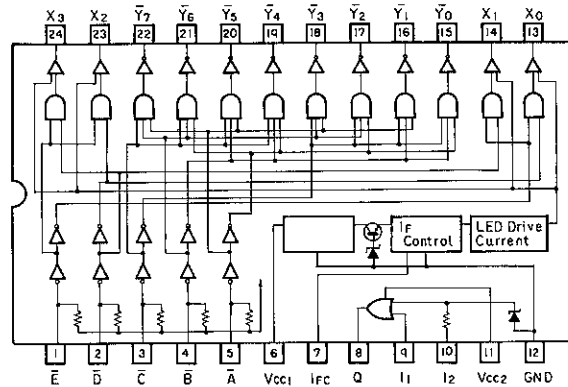
Pin No.	Pin Name	I/O	Standard Voltage (V)				Function and Operation
			PLAY	X2 INPUT	X3 INPUT	X1 INPUT	
5	\overline{DR}	IN	12.7	12.6	12.4	12.4	PLAY running is switched by tape end sensing input. (Pull-up resistor built-in.)
6	CP	OUT	0	10.1	0	0	Pin which drives the direction change solenoid.
7	OF	OUT	0.2	0.2	0.2	3.2	Pin which drives the FF (REW) solenoid.
8	OR	OUT	0.2	0.2	3.2	0	
9	OSC	IN	—	—			Internal clock OSC circuit oscillation frequency setting.
10	\overline{R}	IN					*
11	X3	IN OUT	0	0	12.0	0	FF key input and FF indicator output.
12	X2	IN	0	12.3	0	0	Tape running direction switching. (Pull-down resistor built-in.)
13	X1	IN OUT	0	0	0.2	12.3	REW key input and REW indicator output.
14	\overline{POS}	IN	12.7	12.7	12.4	12.4	
15	\overline{RST}	IN	12.1	12.1	11.9	11.9	IC initial setting input.
16	VDD		12.7	12.7	12.4	12.4	Normally used at 8.0 ~ 16.0V.

* Internal reset pin for POS operation in KP-717G, 818G

(When the automobile main key is turned off in the FF and REW states, the FF and REW state is internally reset by this pin so the PLAY state is always entered when the automobile main key is turned on next.)

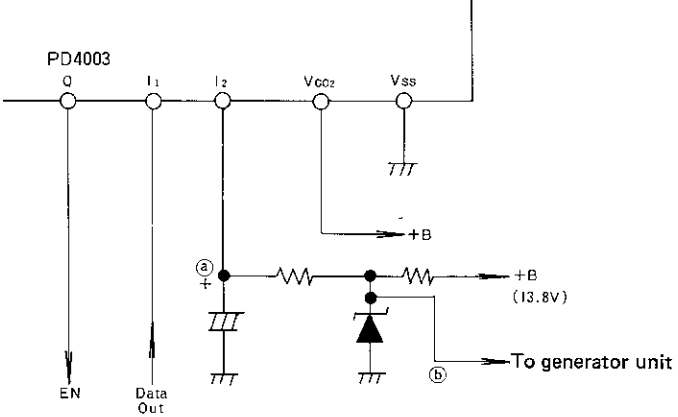
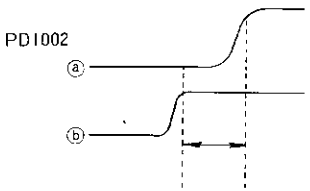
APPLICATION	DIAL DISPLAY DRIVE	NAME	PD 4003
MODEL	GEX-8	TYPE	SILICONE MONOLITHIC BIPOLAR DIGITAL IC

BLOCK DIAGRAM



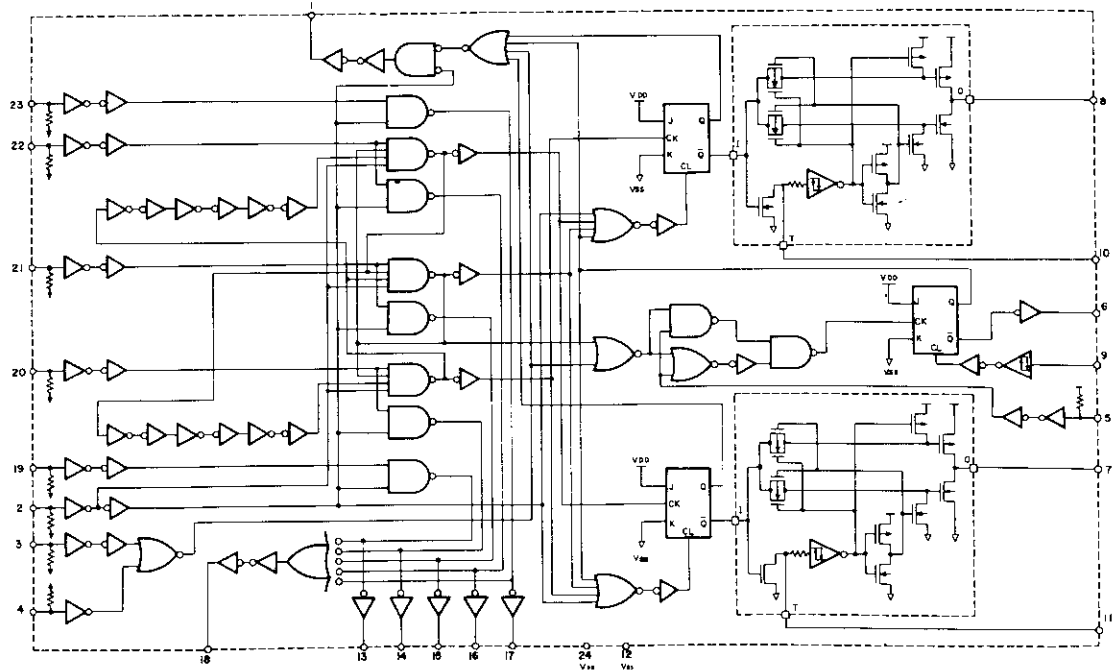
PIN FUNCTIONS

Pin No.	Pin Name	I/O	Function and Operation
1	\bar{E}	IN	$\bar{2} \sim 4$ decoder input terminal. X0 ~ X3 is its output.
2	\bar{D}		
3	\bar{C}	IN	$\bar{3} \sim \bar{8}$ decoder input terminal. $\bar{Y}0 \sim \bar{Y}7$ is its output.
4	\bar{B}		
5	\bar{A}		
6	Vcc1		Power supply. (8.5V)
7	IFC		Intensity adjustment pin. Controls the pins X0 ~ X3 output current. The intensity of the display light emitting diode can be adjusted.
8	Q	OUT	This pin connects directly to the PD1002 enable pin. When the power is turned off, PD1002 Data output becomes Enable "Low" at "Low Level".

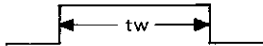
Pin No.	Pin Name	I/O	Function and Operation
9	I1	IN	Connects directly to PD1002 Data Out. Input pin which performs the PD1002 enable operation.
10	I2	IN	<p>+B is applied from the tuner power supply at a suitable time constant.</p>  <p style="text-align: center;">Time difference at power rise</p> 
11	Vcc2		Power supply pin. +B is applied from the same line as the PD1002VDD power supply system. When the power is turned off, this pin is in the power ON state until operation of Q, I1, and I2 (OR circuit) previously described.
12	GND		Power supply pin. Vcc1, Vcc2 common GND.
13	X0	OUT	2 ~ 4 output pins corresponding to decode inputs \bar{E} , \bar{D} . Emitter follower. Output current is performed by IFC. Normally the LED anode is directly connected. Active high.
14	X1		
15	\bar{Y}_0	OUT	$\bar{3} \sim \bar{8}$ decoder output pins corresponding to decoder inputs $\bar{C} \sim \bar{A}$. Open collector. The LED cathod side is directly connected. Active low
16	\bar{Y}_1		
17	\bar{Y}_2		
18	\bar{Y}_3		
19	\bar{Y}_4		
20	\bar{Y}_5		
21	\bar{Y}_6	OUT	$\bar{2} \sim \bar{4}$ output pins corresponding to decode inputs \bar{E} , \bar{D} . Emitter follower. Output current is performed by IFC. Normally the LED anode is directly connected. Active high.
22	\bar{Y}_7		
23	X2		
24	X3		

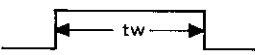
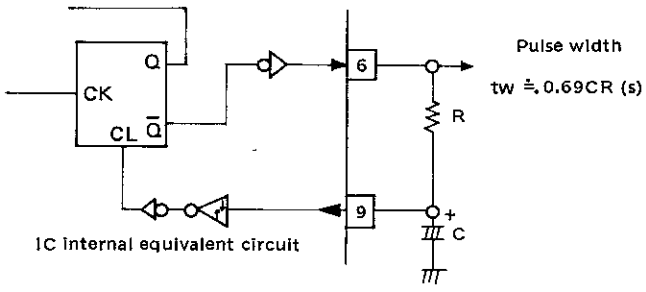
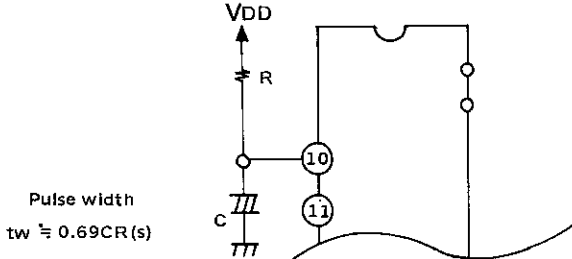
APPLICATION	DECK CONTROL	NAME	PD6002
MODEL	KP-707G	TYPE	C MOS

BLOCK DIAGRAM



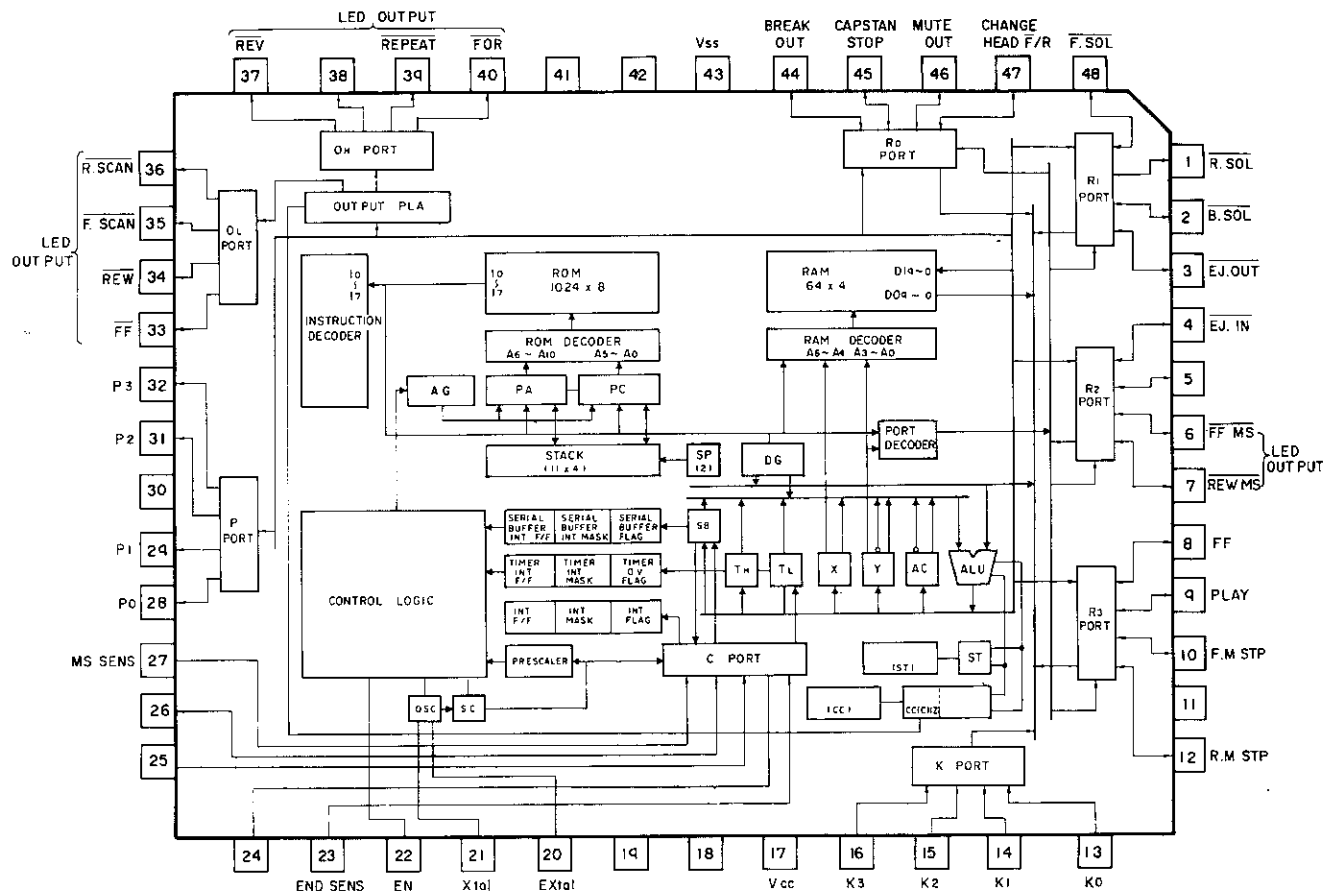
PIN FUNCTIONS

Pin No.	Pin Name	I/O	Function and Operation
1	MI	OUT	Muting output to prevent motor noise during FF/REW.
2	\bar{S}	IN	Switches the tuner function and tape function of sets with an electronic tuner. Used at "H" for tuner and "L" (or open) for tape deck.
3	P	IN	Stop play direction switched by pin ② (x3) during FF/REW. P or \bar{P} is used depending on the motor used in the deck. (1) When P is used, the direction change function is stopped by making \bar{P} open or "H" and P "L" or open. (2) When \bar{P} is used, the direction change function is stopped by making P open or "L" and \bar{P} "H" or open.
4	\bar{P}	IN	
5	\overline{DR}	IN	Switches the play running direction by means of the tape end sensing input. Has priority over all pin modes.
6	OP	OUT	Direction drive output. Output pin to drive the main solenoid.  Pulse width is determined by the external circuit of pin ⑨.

Pin No.	Pin Name	I/O	Function and Operation
7	OF	OUT	FF/REW drive output. Output pin which drives the sub solenoid. (3-STATE OUTPUT)
8	OR	OUT	
9	T1		 <p>Pulse width is determined by the external circuit of pins ⑩ and ⑪.</p> <p>Sets the direction pulse width. Determines the output pulse width of pin ⑥.</p>  <p>Pulse width $tw \approx 0.69CR$ (s)</p> <p>IC Internal equivalent circuit</p>
10	T2		FF/REW output pulse width setting.
11	T3		 <p>Pulse width $tw \approx 0.69CR$ (s)</p>
12	V _{ss}		GND
13	$\overline{Y5}$	OUT	Not used by KP-707G
17	$\overline{Y1}$		
18	M2	OUT	Not used by KP-707G.
19	X5	IN	GND
20	X4		Tape deck control input. Pin ⑳ → REW, Pin ㉑ → Direction, Pin ㉒ → FF
22	X2		
23	X1		GND
24	VDD		+B

APPLICATION	CONTROL IC	NAME	PD6009
MODEL	KP-909G	TYPE	NMOS 4 BIT MICRO COMPUTER

BLOCK DIAGRAM



PIN FUNCTIONS

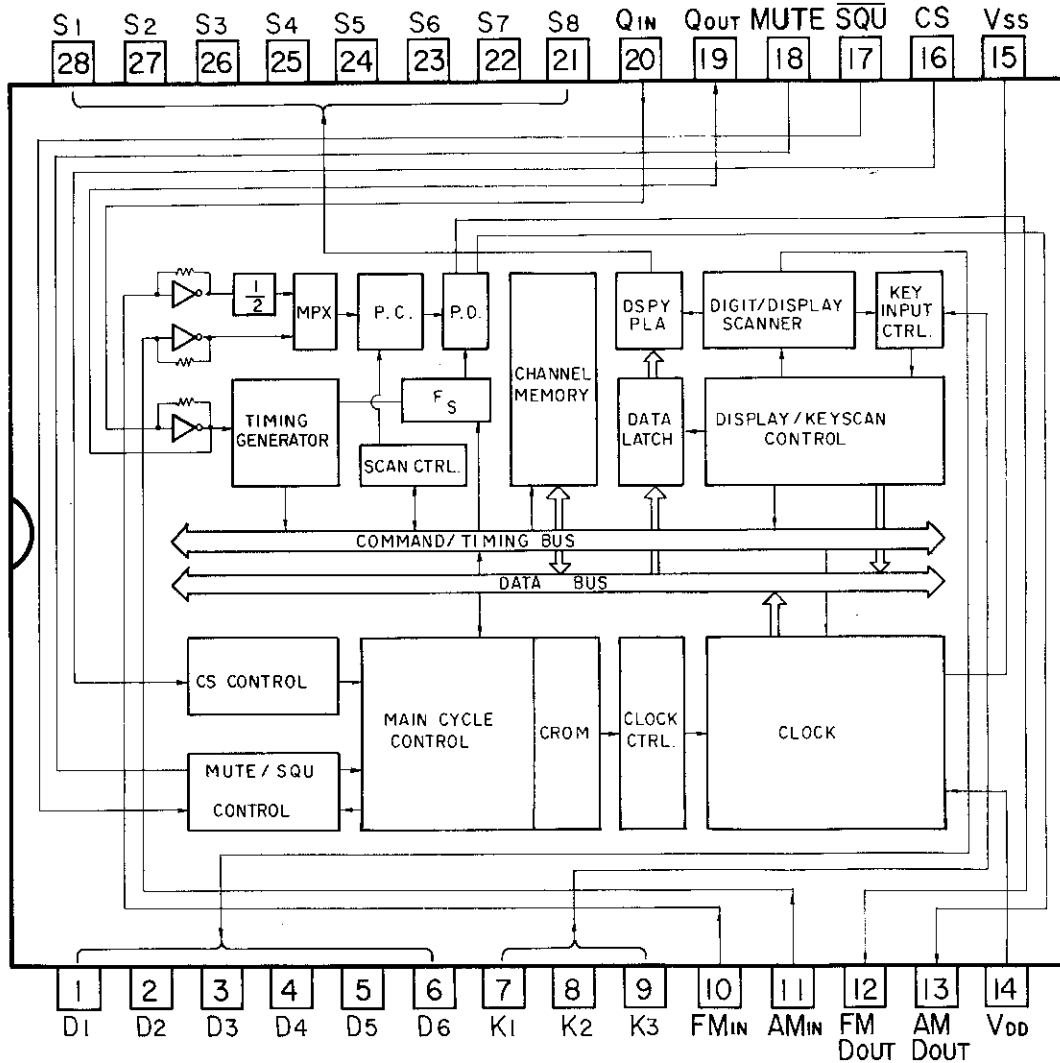
Pin No.	Pin Name	I/O	Function and Operation
1	R.SOL	OUT	Reverse solenoid drive output (HOLD side). Attracted when "L".
2	B.SOL	OUT	Attraction side solenoid drive output (F.R simultaneously). Attracted when "L".
3	EJ.OUT	OUT	Becomes L when eject signal is input from keyboard, etc. to pin 4.
4	EJ.IN	IN	When input when eject signal is "L", makes pin 3 "L". Has priority over all key inputs.
6	F.F.MS	OUT	LED output.
7	REW.MS	OUT	LED output.
8	F.F	OUT	Accelerates the reel motor in the F.F (REW) state when "H".
9	PLAY	OUT	P/F.F, MS pin. Switches the reel motor servoamp at PLAY and F.F, MS. PLAY when "H".

Pin No.	Pin Name	I/O	Function and Operation
10	F. M STP	OUT	Stops the forward side reel motor. STOP when "H".
12	R. M STP	OUT	Stops the reverse side reel motor. STOP when "H".
13	K0	IN	FWD-SCAN, REV-SCAN
14	K1		REW, REPEAT, BLANK SKIP
15	K2		FF, RELEASE
16	K3		PAUSE
			} Key matrix input
17	Vcc		5V ±0.5V
20, 21	Extal, X'tal	IN	Clock 3.00MHz ±0.2%
22	EN		Terminal which starts the system. Start when "H". All output pins made "H" when "L".
23	END SENS	IN	End sensing input. End is sensed when no pulse input state continues for 1 second or longer.
27	MS. SENS	IN	MS sensing input. The interselection sensing pulse is input. Interselection is assumed when no pulse input state continues for 3 second or longer during PLAY.
28	P0	OUT	FF, REW, REV-SCAN
29	P1		RELEASE, REPEAT, FWD-SCAN
31	P2		PAUSE, BLANK SKIP
			} Key scan output
33	F. F	OUT	LED output.
34	REW	OUT	LED output.
35	F. SCAN	OUT	LED output.
36	R. SCAN	OUT	LED output.
37	REV	OUT	LED output.
39	REPEAT	OUT	LED output.
40	NOR	OUT	LED output.
43	Vss		GND
44	BREAK OUT	OUT	Break key signal output. Break signal is output at the reel motor when "H".
45	CAPSTAN STOP	OUT	Capstan motor stop pin. STOP when "H".
46	MUTE OUT	OUT	Muting output. Muting applied when "H".
47	CHANGE HEAD F/R.	OUT	Forward/reverse signal switching output. Forward side when "L".
48	F. SOL	OUT	Forward solenoid drive output (HOLD side). Attracted when "L".

Family	Comparison
PD6009A	Addition of muting output when stopping.

APPLICATION	PLL SYNTHESIZER	NAME	PD7001
MODEL	KE-5000/U. C	TYPE	C MOS

BLOCK DIAGRAM

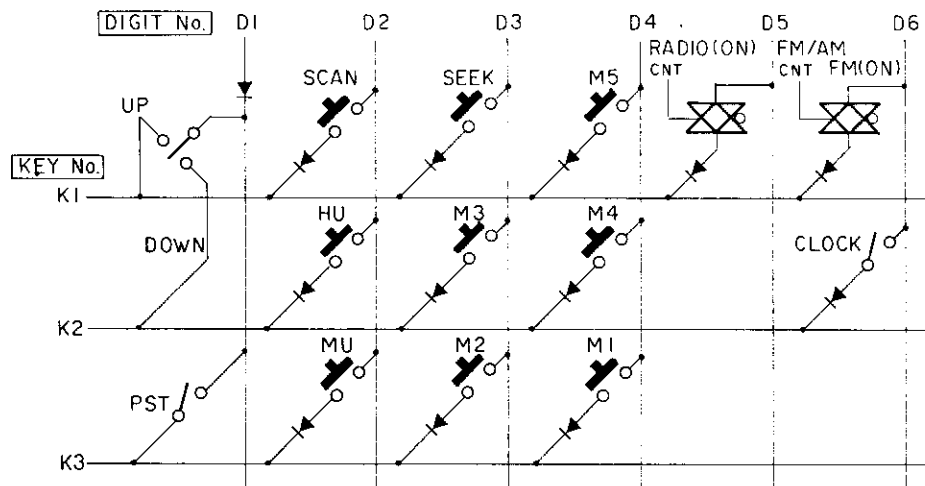


PIN FUNCTIONS

Pin No.	Pin Name	I/O	Function and Operation
1 ~ 6	D1 ~ D6	OUT	Display digit drive output/key scan output. Active "H".

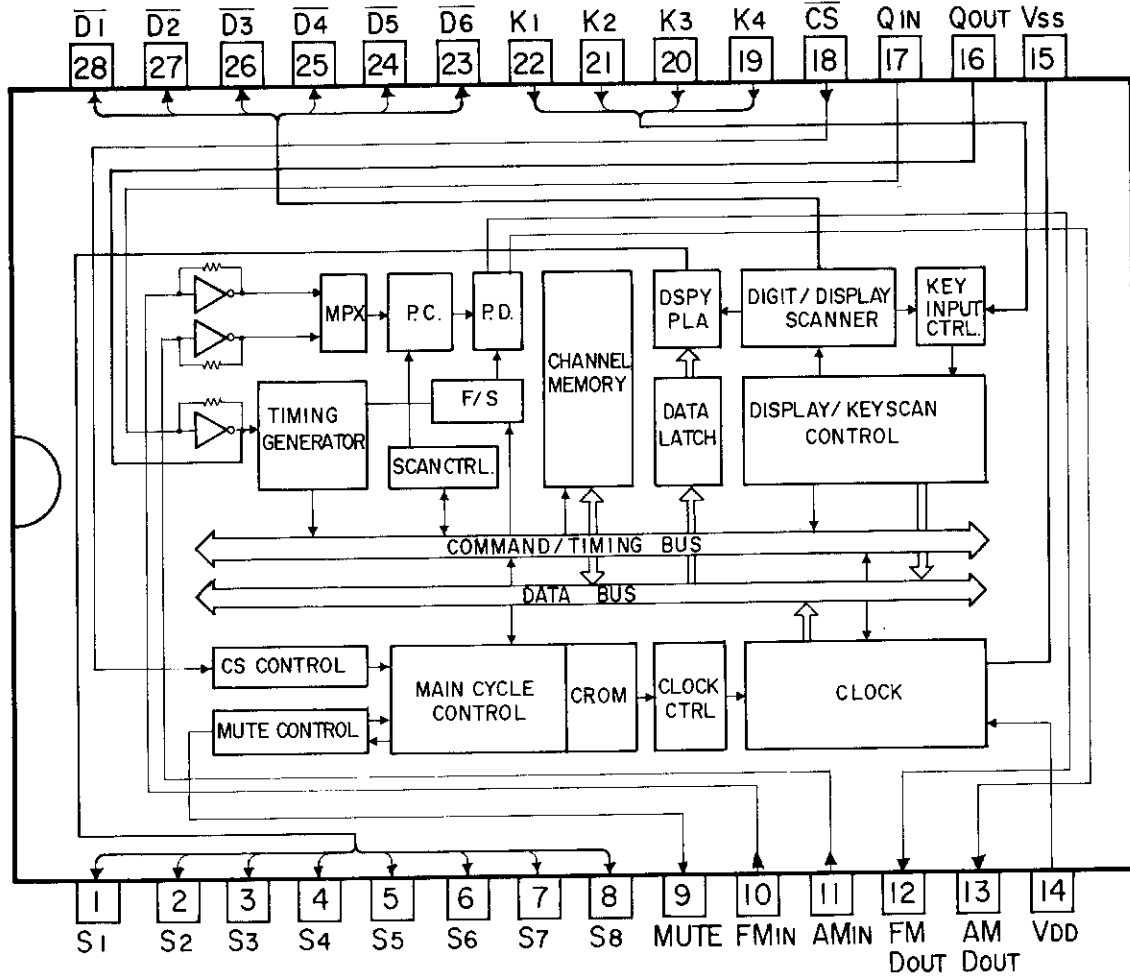
Pin No.	Pin Name	I/O	Function and Operation
7 ~ 9	K1 ~ K3	IN	Key sense input. Pull-down resistor built-in.
10	FM IN	IN	FM station input.
11	AM IN	IN	AM station input.
12	FM DO	OUT	FM phase comparison output. High impedance at AM.
13	AM DO	OUT	AM phase comparison output. High impedance at FM.
14	VDD		Power supply. (+B, normally 5V)
15	Vss		Power supply. Common ground.
16	CS	IN	Chip select input. Key input inhibited when "L". Pull-up resistor built-in.
17	SQU	IN	Squelch input. Scanning stop when "L".
18	MUTE	OUT	Muting output. Appropriate muting during station selection.
19	Q OUT	OUT	5.12 MHz crystal oscillator output.
20	Q IN	IN	5.12 MHz crystal oscillator input.
21 ~ 28	S1 ~ S8	OUT	Display segment drive output. Active "H".

KEY MATRIX



APPLICATION	PLL SYNTHESIZER	NAME	PD7002
MODEL	KE-5000/E	TYPE	C MOS

BLOCK DIAGRAM

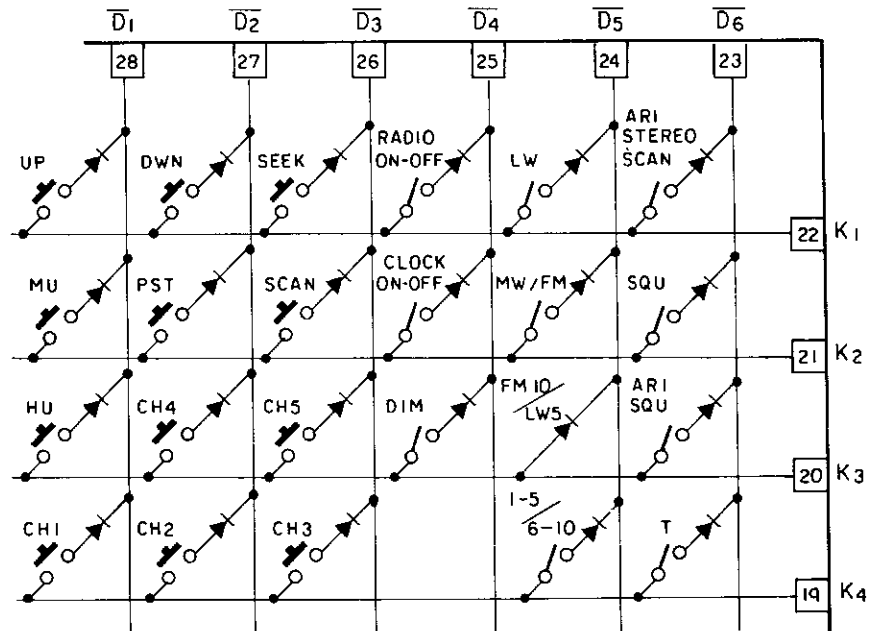


PIN FUNCTIONS

Pin No.	Pin Name	I/O	Function and Operation
1 ~ 8	S1 ~ S8	OUT	Display segment drive output. Active "H".
9	MUTE	OUT	Muting output terminal. Appropriate muting during station selection.
10	FM IN	IN	FM station input.

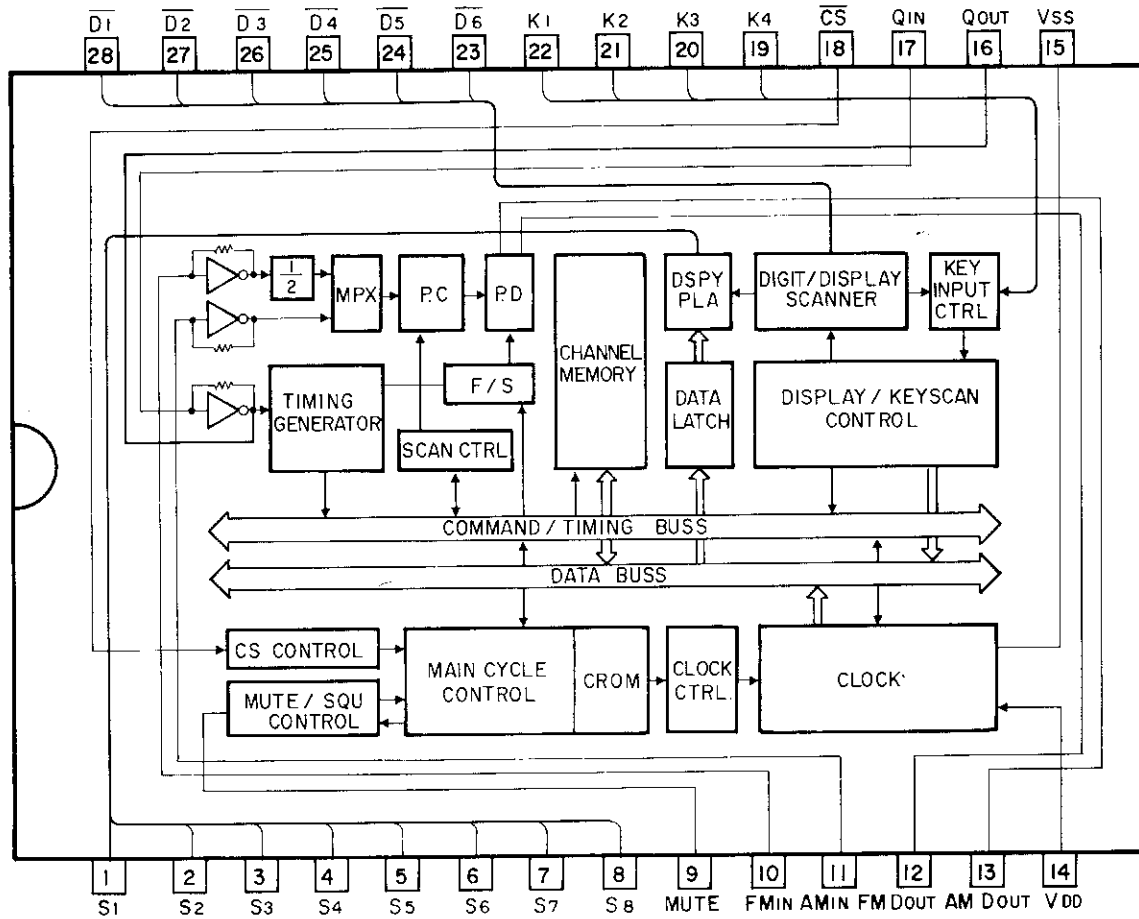
Pin No.	Pin Name	I/O	Function and Operation
11	AM IN	IN	AM station input.
12	FM DO	OUT	FM phase comparison output. High impedance at AM.
13	AM DO	OUT	AM phase comparison output. High impedance at FM.
14	VDD		Power supply. Normally 5V.
15	VSS		Power supply. Common ground.
16	Q OUT	OUT	4.5MHz crystal oscillator output.
17	Q IN	IN	4.5MHz crystal oscillator input.
18	\overline{CS}	IN	Chip select input. Key input inhibited when "L" or open. Pull-down resistor built-in.
19 ~ 22	K1 ~ K4	IN	Key sense input. Pull-up resistor built-in.
23 ~ 28	$\overline{D1} \sim \overline{D6}$	OUT	Display digit drive output/key scan output. Active "L".

KEY MATRIX



APPLICATION	PLL SYNTHESIZER	NAME	PD7003
MODEL	GEX-90/US. CA	TYPE	C MOS

BLOCK DIAGRAM



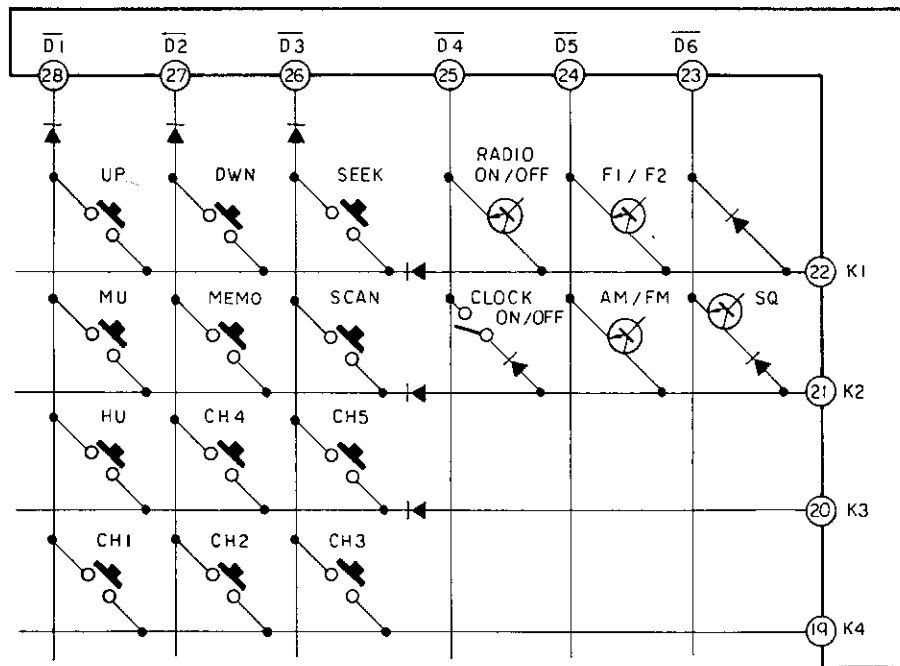
PIN FUNCTIONS

Pin No.	Pin Name	I/O	Function and Operation
1 ~ 8	S1 ~ S8	OUT	Display segment drive output. Active "H".
9	MUTE	OUT	Muting output during station selection.
10	FM IN	IN	FM station input.
11	AM IN	IN	AM station input.
12	FM DO	OUT	FM phase comparison output. High impedance at AM.
13	AM DO	OUT	AM phase comparison output. High impedance at FM.

Pin No.	Pin Name	I/O	Function and Operation
14	VDD		Power supply. +5V
15	Vss		Power supply. Common ground.
16, 17	Q, OUT, Q IN		4.5MHz crystal oscillator output, input.
18	\overline{CS}	IN	Chip select input. Key input inhibited when CS = "L" or open. Tuner operation when CS = "H".
19 ~ 22	K1 ~ K4	IN	Key scan input. Pull-up resistor built-in.
23 ~ 28	$\overline{D1} \sim \overline{D6}$	OUT	Display digit drive output. Key scan output. Active "L".

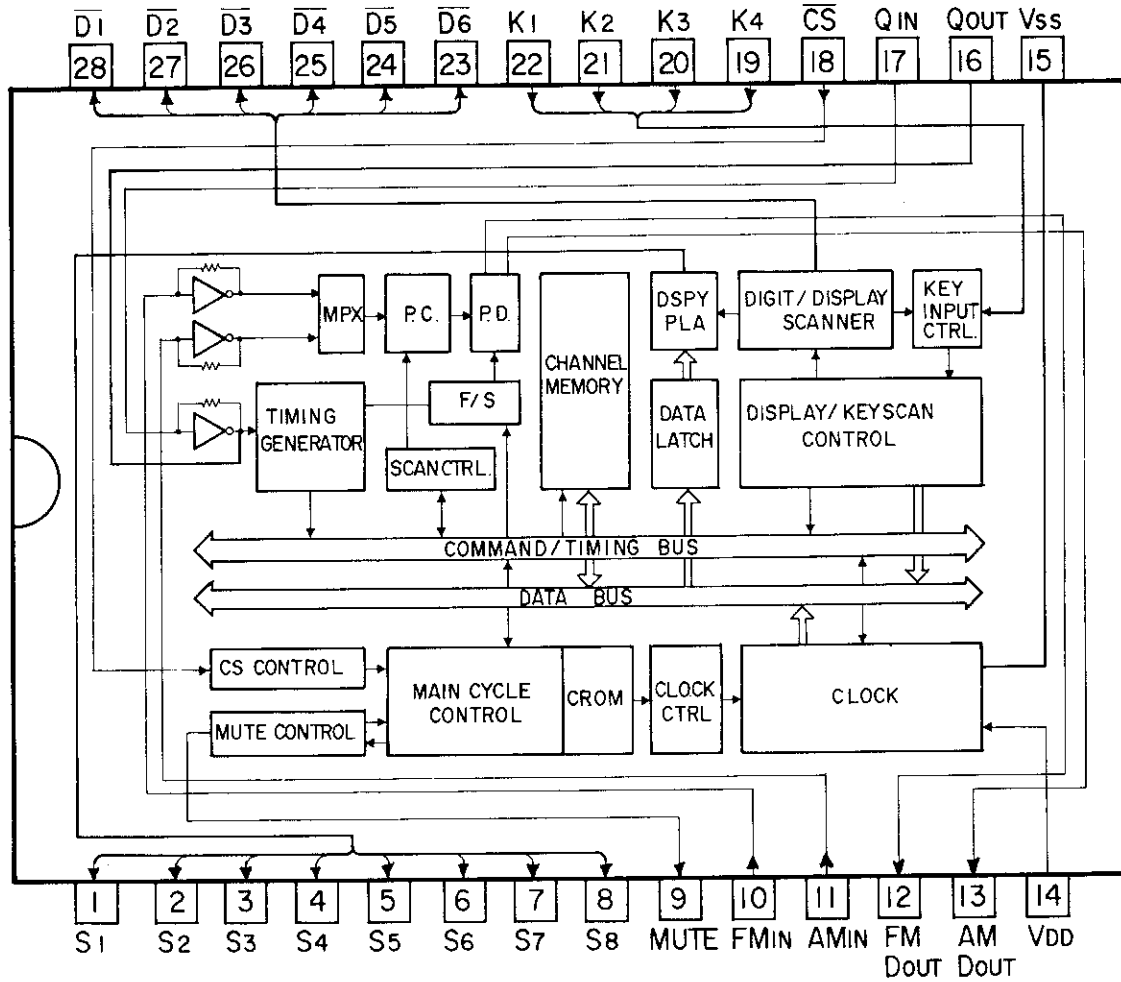
Family	Comparison
PD7003A	7003 data lock countermeasures.
PD7003B	7003A cost reduction.

KEY MATRIX



APPLICATION	PLL SYNTHESIZER	NAME	PD7004
MODEL	KEX-70/E	TYPE	C MOS

BLOCK DIAGRAM

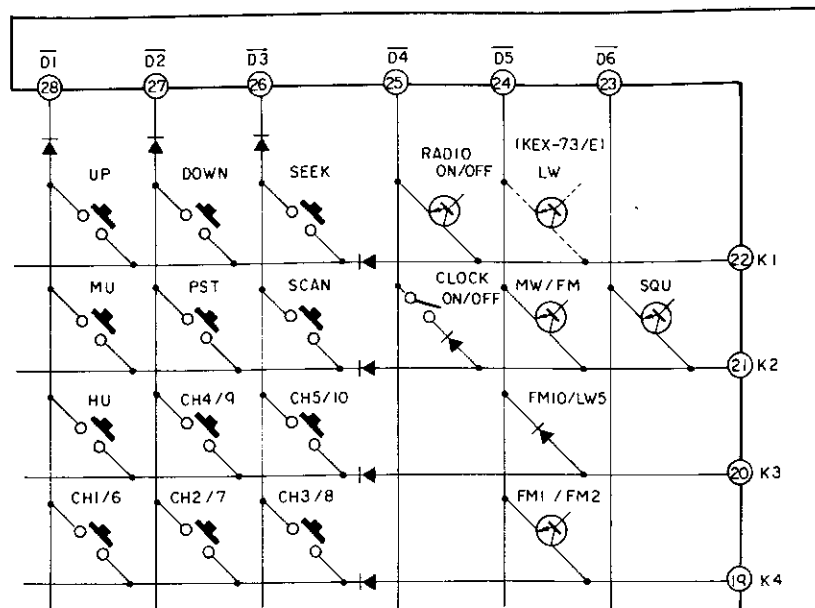


PIN FUNCTIONS

Pin No.	Pin Name	I/O	Function and Operation
1 ~ 8	S1 ~ S8	OUT	Display segment drive output. Active "H".
9	MUTE	OUT	Muting output. Appropriate muting during station selection.
10	FM IN	IN	FM station input.

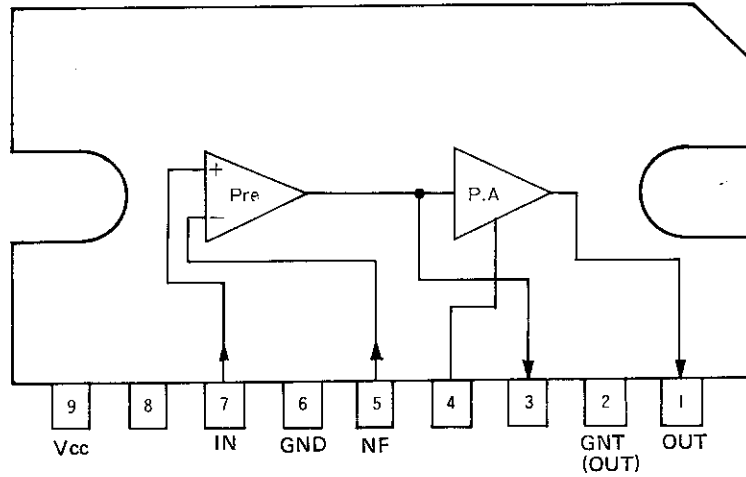
Pin No.	Pin Name	I/O	Function and Operation
11	AM IN	IN	AM station input.
12	FM DO	OUT	FM station comparison output. High impedance at AM.
13	AM DO	OUT	AM phase comparison output. High impedance at FM.
14	VDD		Power supply. Normally 5V.
15	VSS		Power supply. Common ground.
16	Q OUT	OUT	4.5MHz crystal oscillator output.
17	Q IN	IN	4.5MHz crystal oscillator input.
18	\overline{CS}	IN	Chip select input. Key input inhibited when "L" or open. Pull-down resistor built-in.
19 ~ 22	K1 ~ K4	IN	Key sense input. Pull-up resistor built-in:
23 ~ 28	$\overline{D1} \sim \overline{D6}$	OUT	Display digit drive output/key scan output. Active "L".

KEY MATRIX



APPLICATION	POWER AMP	NAME	AN214
MODEL	KP-292	TYPE	SILICONE MONOLITHIC BIPOLAR LINEAR IC

BLOCK DIAGRAM

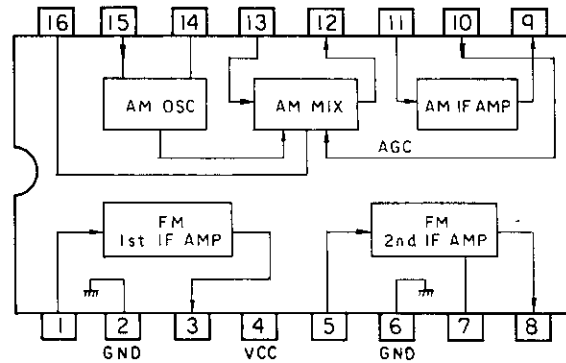


PIN FUNCTIONS

Pin No.	Standard Voltage (V)	I/O	Function and Operation
1	6.1	OUT	Output
2	0		Ground (output)
3	7.4		Oscillation prevention.
4	10.9		Boot strap
5	6.0		Negative feedback (NF).
6	0		GND
7	6.0	IN	Noninverting input.
8	12.3		Ripple filter.
9	13.8		Vcc

APPLICATION	FM/AM IF AMP	NAME	AN366
MODEL	RK-306	TYPE	SILICONE MONOLITHIC BIPOLAR LINEAR IC

BLOCK DIAGRAM



PIN FUNCTIONS

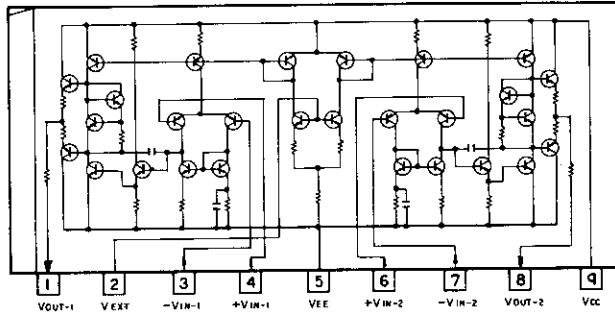
Pin No.	Standard Voltage (V)	I/O	Function and Operation
1	0.8	IN	FM IF input (1st)
2	0		GND (input)
3	2.2	OUT	FM IF output (1st)
4	4.9		Vcc
5	1.3	IN	FM IF input (2nd)
6	0		GND (output)
7	1.3		Bypass
8	4.8	OUT	FM IF output (2nd)
9	0.8 (5.1)	OUT	AM IF output
10	0.8(1.4)	IN	AM AGC input
11	0.8	IN	AM IF input
12	0.8(0.5)	OUT	AM MIX output
13	0.4(0.7)	IN	AM RF input
14	0.8(1.8)		AM MIX AGC
15	0.8(4.3)	IN	AM OSC input
16	0		Bypass

(V): At AM

AN

APPLICATION	DUAL OPERATIONAL AMPLIFIAR	NAME	AN6550
MODEL	SK-700	TYPE	SILICONE MONOLITHIC BIPOLAR LINEAR IC

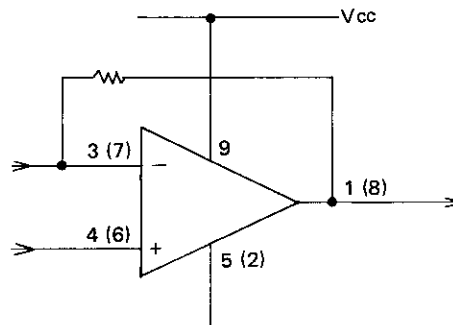
BLOCK DIAGRAM



PIN FUNCTIONS

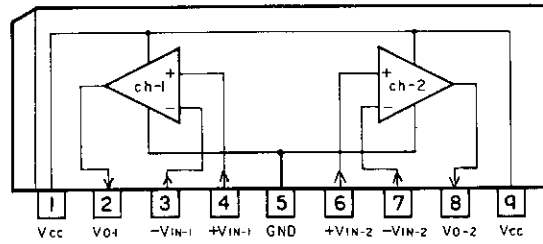
Pin No.	Standard Voltage (V)	I/O	Function and Operation
1	5.2	OUT	ch-1
2	5.9		Vcc (EXT)
3	5.2	IN	(-) ch-1
4	5.2	IN	(+) ch-1
5	0		GND
6	5.2	IN	(+) ch-2
7	5.2	IN	(-) ch-2
8	5.2	OUT	ch-2
9	10.4		Vcc

CONNECTION DIAGRAM



APPLICATION	DUAL CONPARATOR	NAME	AN6913
MODEL	SK-700	TYPE	SILICONE MONOLITHIC BIPOLAR LINEAR IC

BLOCK DIAGRAM

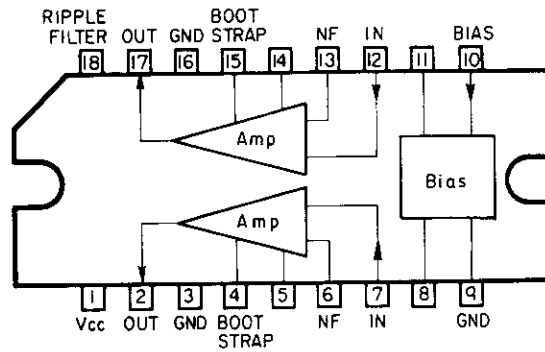


PIN FUNCTIONS

Pin No.	Standard Voltage (V)	Function and Operation
1	7.0	Vcc
2	0.7	Output (ch-1)
3	3.8	(-) input (ch-1)
4	4.2	(+) input (ch-1)
5	0	GND
6	3.8	(+) input (ch-2)
7	3.4	(-) input (ch-2)
8	0.7	Output (ch-2)
9	7.0	Vcc

APPLICATION	POWER IC	NAME	AN7146M
MODEL	SK-51	TYPE	SILICONE MONOLITHIC BIPOLAR LINEAR IC

BLOCK DIAGRAM

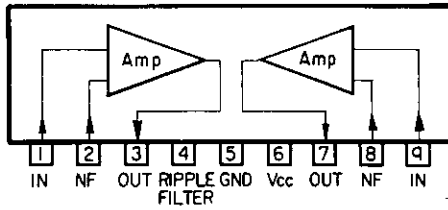


PIN FUNCTIONS

Pin No.	Standard Voltage (V)	I/O	Function and Operation
1	13.5		Vcc
2	7.1	OUT(L)	Output (ch-1)
3	0		GND (ch-1, output side)
4	12.0		Boot strap (ch-1)
5	1.5		Oscillation prevention (ch-1)
6	3.5		Negative feedback (ch-1)
7	3.5	IN(L)	Input (ch-1)
8			(Used at BTL)
9	0		GND (both chs, input side)
10	3.6		Input bias (both chs)
11			(Used at BTL)
12	3.5	IN(R)	Input (ch-2)
13	3.5		Negative feedback (ch-2)
14	1.5		Oscillation prevention (ch-2)
15	12.0		Boot strap (ch-2)
16	0		GND (ch-2, output side)
17	7.1	OUT(R)	Output (ch-2)
18	13.0		Ripple filter

APPLICATION	DUAL PREAMP	NAME	AN7311
MODEL	SK-51	TYPE	SILICONE MONOLITHIC BIPOLAR LINEAR IC

BLOCK DIAGRAM

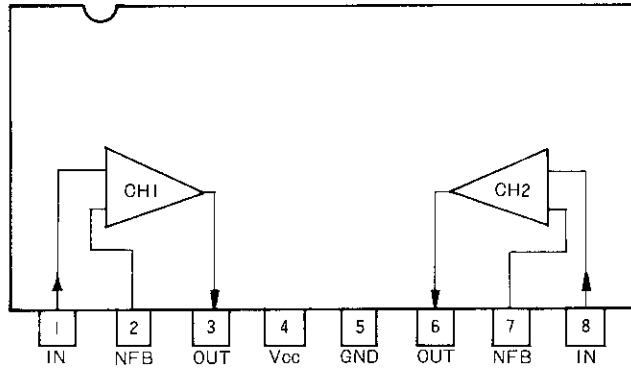


PIN FUNCTIONS

Pin No.	Standard Voltage (V)	I/O	Function and Operation
1	1.3	IN	Input (ch-1)
2	0.7		Negative feedback (ch-1)
3	4.2	OUT	Output (ch-1)
4	4.9		Filter
5	0		GND
6	11.0		Vcc
7	4.2	OUT	Output (ch-2)
8	0.7		Negative feedback (ch-2)
9	1.3	IN	Input (ch-2)

APPLICATION	DUAL PREAMP	NAME	BA328
MODEL	KH-2277	TYPE	SILICONE MONOLITHIC BIPOLAR LINEAR IC

BLOCK DIAGRAM

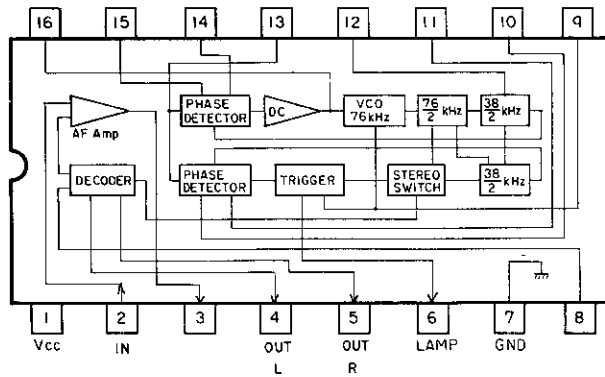


PIN FUNCTIONS

Pin No.	Standard Voltage (V)	I/O	Function and Operation
1	1.4	IN	Input (ch-1)
2	0.9		Negative feedback (ch-1)
3	4	OUT	Output (ch-1)
4	15.1		Vcc
5	0		GND
6	4	OUT	Output (ch-2)
7	0.9		Negative feedback (ch-2)
8	1.4	IN	Input (ch-2)

APPLICATION	PLL TYPE FM MULTIPLIX STEREO DEMODULATOR	NAME	BA1320
MODEL	RH-4411	TYPE	SILICONE MONOLITHIC BIPOLAR LINEAR IC

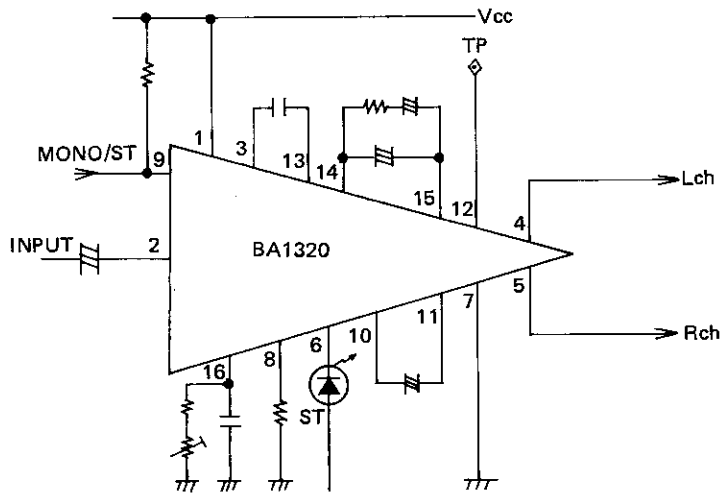
BLOCK DIAGRAM



PIN FUNCTIONS

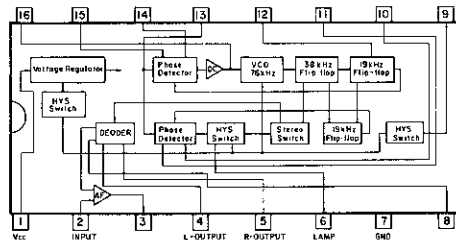
Pin No.	Standard Voltage (V)	I/O	Function and Operation
1	14		Vcc
2	2.8	IN	Input
3	2.8		AF AMP output
4	6.2	OUT	Output (Lch)
5	6.2	OUT	Output (Rch)
6			Stereo indicator
7	0		GND
8			Separation control
9	1.6/0		MONO/ST
10	2.2		Low-pass filter
11	2.2		Low-pass filter
12	0.4		Test point (19kHz)
13	2.2	IN	Detector input.
14	2.2		Loop filter
15			Loop filter
16			19kHz adjustment pin

CONNECTION DIAGRAM

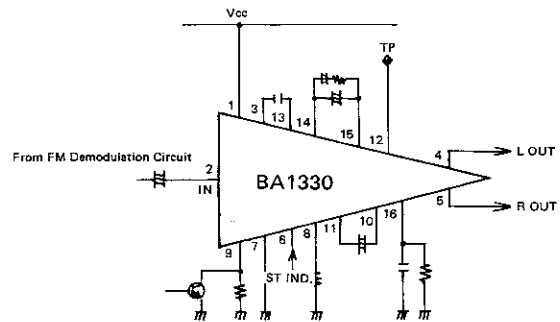


APPLICATION	FM MPX STEREO DEMODULATION	NAME	BA1330
MODEL	SK-200	TYPE	SILICONE MONOLITHIC BIPOLAR LINEAR IC

BLOCK DIAGRAM



CONNECTION DIAGRAM

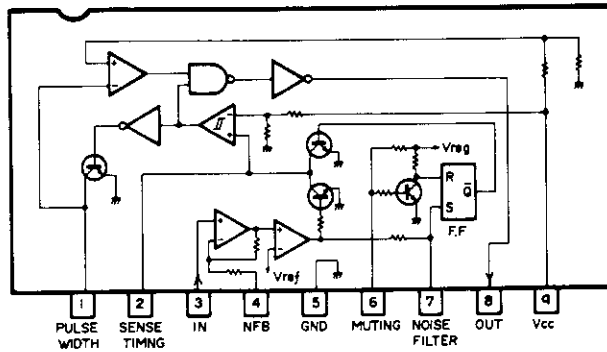


PIN FUNCTIONS


Pin No.	Standard Voltage (V)	I/O	Function and Operation
1	6.18		Vcc
2	1.86	IN	Composite input
3	2.22	OUT	Composite output
4	3.01	OUT	Lch output
5	3.04	OUT	Rch output
6	5.15/0.69		Lamp (MONO/ST)
7	0		GND
8	0.49		Separation control
9	2.5/0.03		VCO STOP (2.5V)
10	1.45		Low-pass filter
11	1.45		Low-pass filter
12	0.16		19kHz monitor
13	1.45	IN	Loop input
14	1.45		Loop filter
15	1.45		Loop filter
16	2.82		19kHz frequency control

APPLICATION	INTERSELECTION DETECTION END DETECTION	NAME	BA338
MODEL	KP-404G	TYPE	SILICONE MONOLITHIC BIPOLAR DIGITAL IC

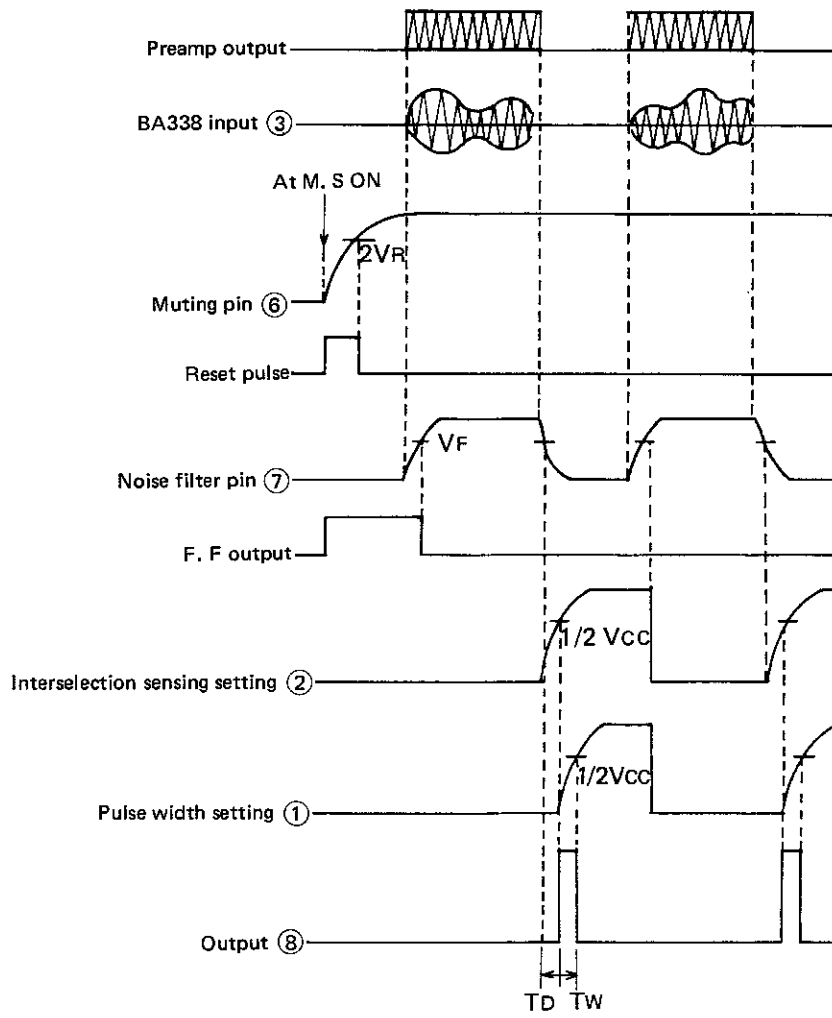
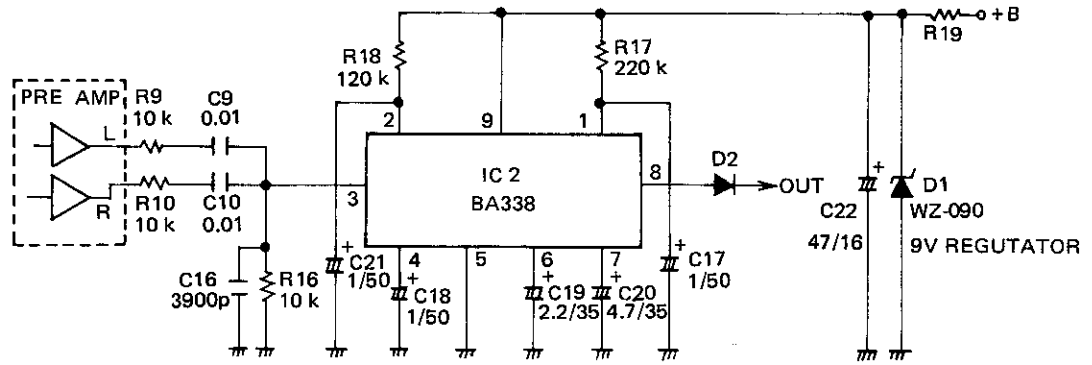
BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Standard Voltage (V)	I/O	Function and Operation
1	0		Output pulse width setting
2	0.5		Interselection sensing time setting
3	0	IN	Input
4	1		Negative feedback
5	0		GND
6	1.6		Muting (MS inhibited at power ON)
7	0.6		Noise filter
8	8.0	OUT	Output 
9	9.1		Vcc

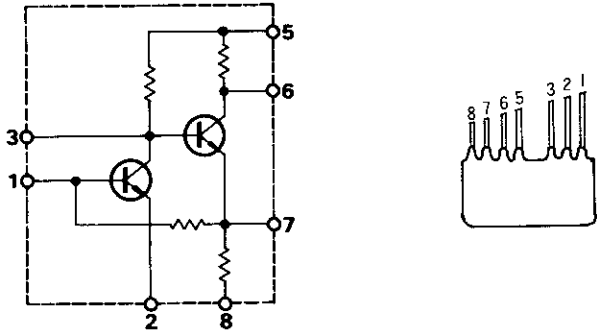
CONNECTION DIAGRAM



TD: Intersession sensing time
 TW: Intersession sensing pulse width

APPLICATION	PRE AMP	NAME	FA6013D
MODEL	KP-333	TYPE	HYBRID IC

BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Standard Voltage (V)	I/O	Function and Operation
1	0.6	IN	Audio input
2	0.04		Negative feedback
3	1.4		
4	/	/	Deleted
5	9.3		Vcc
6	5.8	OUT	Audio output
7	0.3		Bypass capacitor use
8	0		GND